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Low-power Wake-up Receiver with Subthreshold CMOS Circuits for Wireless Sensor Networks

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Abstract— We developed a wake-up receiver comprised of subthreshold CMOS circuits. The proposed receiver includes an envelope detector, a high-gain baseband amplifier, a clock and data recovery (CDR) circuit, and a wake-up signal recognition circuit. The drain nonlinearity in the subthreshold region effectively detects the baseband signal with a microwave carrier. The offset cancellation method with a biasing circuit operated by the subthreshold produces a high gain of more than 100 dB for the baseband amplifier. A pulse-width modulation (PWM) CDR drastically reduces the power consumption of the receiver. A 2.4-GHz detector, a high-gain amplifier and a PWM clock recovery circuit were designed and fabricated with 0.18-μm CMOS process with one poly and six metal layers. The fabricated detector and high-gain amplifier achieved a sensitivity of −47.2 dBm while consuming only 6.8 μW from a 1.5 V supply. The fabricated clock recovery circuit operated successfully up to 500 kbps.

Keywords: Wake-up receiver, envelope detector, high-gain amplifier, clock and data recovery, subthreshold operation

1. Introduction

Reducing power consumption is a key issue in the development of ubiquitous wireless networks. Among all the sensor node functions, such as computation, sensing, and actuation, wireless communication energy is still a dominant component. Ideally, the energy for ubiquitous wireless components should be supplied with micro-miniature batteries or energy harvested from the environment [1]. The sensor network components must be able to sustain long-term operation while using only limited power sources (< a few μW). The technical challenge in coming up with strong enough components is developing sensor LSIs that can operate using extremely limited electricity [2]. Wake-up receivers have previously been proposed [3]–[5] to reduce the power consumption of sensor LSIs.

When a wake-up signal from a master (control) node is received, the wake-up receiver activates other parts of the sensor LSI in sleep mode. Because it operates continuously, it is important that the wake-up receiver does not consume much power. Conventional detectors such as those using super-heterodyne architecture are problematic because they consume most of the energy in the mixer and local oscillator (LO). A direct (envelope) detection system with high-gain baseband amplifiers has been proposed as an alternative architecture [5]. However, a baseband clock recovery circuit for a low data rate (10–100 kbps) is difficult to monolithically integrate on a CMOS chip due to the large passive elements.

In this paper, we propose a low power wake-up receiver with CMOS operating in the subthreshold current region. The main features of the wake-up receiver are:

(1) A direct-detection circuit using the nonlinearity of the drain current in the subthreshold region.

(2) A high-gain baseband amplifier with offset canceller biased in the subthreshold region.

(3) An all-digital, data-rate-independent clock and data (CDR) recovery for a pulse-width-modulated (PWM) wake-up signal.

2. Architectures of wake-up receiver

A low-rate (10–100 kbps) PWM signal was used for the wake-up signal with a carrier frequency of 2.4 GHz. The block diagram of the wake-up receiver is shown in Fig. 1. The receiver consists of the envelope detector, high-gain baseband amplifier, PWM CDR, and code recognition circuit. A direct-detection receiver suffers from erroneous wake-up due to noise and interferences caused by other wireless devices in the same frequency band. In order to avoid this erroneous wake-up, (1) the PWM signal was used for perceiving modulated signals from other devices as background noise than interferers and (2) the wake-up signal contained a length of address code [5]. Here, we focus on the detector, high-gain amplifier, and PWM CDR. A detailed system-level discussion on the wake-up signal format is beyond the scope of this paper.

2.1 Detector

A common amplifier [6], shown in Fig. 2, was used for both the detector and the baseband amplifier. The feedback circuit consists of subthreshold op amps. The input-/output-voltages are fixed to the common-mode voltage V_{CM} at the DC level. The subthreshold op amps operate very slowly with a large time constant, so the feedback operation is established only at DC and very low frequencies (below 10 Hz). The differential amplifier operates as a high-pass filter and therefore shows no DC offset in its output. ('DC offset' is the sum of an offset due to mismatches in the differential M3–M6 pair and an offset due to the DC component of the differential input signal.) The differential amplifier operates with a very small tail current I_0 (< 1 nA), and MOSFETs in the input stage are therefore biased in the subthreshold region. The envelope detection was performed with the nonlinearity of drain current in the subthreshold region. The p-MOS was used as a driving MOSFET M2 to decrease the 1/*f* noise.

Although the carrier frequency is high (2.4 GHz), a low-rate baseband signal can be detected even when the detector is biased in the subthreshold region. The drain current responds instantaneously to variation of the gate-voltage V_{GS} of the MOSFET M2 (Fig. 2).

2.2 High-gain amplifier

The circuit in Fig. 2 operates as an amplifier at the baseband frequency signal. A directly coupled amplifier with an extremely high gain of more than 100 dB is difficult to achieve due to the DC offset problem. The amplifier shown in Fig. 2 solved this problem. Without the subthreshold operated feedback circuit, a DC output offset would be produced and amplified with a high gain to saturate the output of the amplifier. In practice, owing to the feedback through the subthreshold op amps, the output offset is set to 0 and the common-mode level is fixed to V_{CM} regardless of device properties and mismatches. (Strictly speaking, a slight offset voltage equal to the input-referred offset voltage of the subthreshold op amps appears in the output.) The high gain amplifier with this offset cancellation circuit has no DC gain but can normally amplify AC input signals.

2.3 PWM clock and data circuit

The PWM signal has a baseband clock component in its frequency spectrum that can simplify the clock recovery circuit. This is why we chose PWM for the wake-up signal. Figure 3 shows a block diagram and an example timing chart of the PWM CDR circuit we developed.

The operation sequence of the PWM CDR is as follows.

(1) When a wake-up signal arrives at the CDR, the turn-on detection circuit activates the ring oscillator (OSC), resets the counter, and transfers the content of the counter to the register. The oscillation frequency of the ring oscillator is designed to be at least four times higher than the baseband frequency.

(2) A 1-bit shifted (1/2) value of the counted number (= the number of oscillator pulses in one time slot) is transfered to the register. When the contents of the counter and the register coincide with each other, the clock becomes “high.” Othewise, it is “low.” This means that the clock turns on at the center position of the time slot. At this moment, the data is read by using the clock and a value of “1” or “0” is registered in the D-F/F.

(3) When the wake-up signal stops and the counter overflows, the ring oscillator is turned off.

The main advantage of the PWM CDR circuit over conventional CDRs is that no exact relationship is required between the oscillation frequency and the baseband frequency. In addition, the CDR is an all-digital circuit and its average power consumption is almost 0 because it only operates when a wake-up signal is input.

3. Design and fabrication

We designed and fabricated the envelope detector and high-gain baseband amplifier in a 0.18-μm mixed signal/RF CMOS process with one poly and six metal layers. Figure 4 shows the schematic of the detector and the baseband amplifier. Here, the “Amp.” is the same as the circuit shown in Fig. 2. We designed an LC matching circuit at 2.4 GHz of the carrier frequency by using an ADS circuit simulator. The total gain of the 3-stage amplifiers using HSPICE was about 115 dB in the frequency range of 1–100 kHz. A MOSFET M8 was used as a current mirror circuit that determined the drain current of the drive MOSFET (M2) in the detector. The center voltage V_{CM} of the detector (1-stage Amp.) and high-gain amp (2-stage Amp.) were produced by this circuit. The V_{CM2} of the 3-stage Amp. was determined by the ratio of the R3 and R4 resistors. The supply voltage V_{dd} and V_{CM2} were designed to be 1.5 and 0.75 V, respectively. External resistors were used for R2−R4 to vary the current in the gain stages and V_{CM2}. For simplicity, the gate of the current source transistor M7 shown in Fig. 2 was grounded. It is of concern, however, that the circuit performance is affected by variations in fabrication parameters and ambient temperature. Figure 5(a) shows the simulated gain characteristics for the amplifiers at 25° C. The higher cutoff was dominated by the gain stage (M1 and M2 in Fig. 2), while the lower cutoff was determined by the subthreshold op amp. A faster p-MOS increased the current I_0 and the cutoff frequency of the op amp. Figure 5(b) shows the simulated effect of the ambient temperature on the gain characteristics for the amplifiers with typical fabrication parameters. Elevated temperature degraded the gain characteristics in the low frequency region. A low-power current reference circuit with temperature and process compensation should be introduced in practical use of the amplifiers [7]. Although the detector and amplifiers were designed at V_{dd} = 1.5 V for battery operation, transient circuit simulations suggested that these circuits operated even at V_{dd} = 1 V. The fabricated detector and high-gain amplifier without an LC matching circuit was 290 μm × 300 μm (Fig. 6). Its total size was 810 μm × 800 μm.

In addition to the detector and high-gain amplifier, we designed and fabricated a PWM clock recovery circuit with the same CMOS process. The designed oscillation frequency of the ring oscillator was about 2

MHz. The counter had 23 stage T-F/Fs. The fabricated PWM clock recovery circuit was 420 μm × 110 μm (Fig. 7).

4. Measurement results

We measured the chip by on-wafer probing with a commercial battery. The measured input return loss (S_{11} parameter) showed that the impedance matching frequency shifted from the designed value of 2.4 GHz to around 1.75 GHz (as shown in Fig. 8). Circuit simulations revealed that this shift was caused by the wiring and pad not being taken into account during the design phase. The measurement of the detector and amplifier was then performed again with 1.75 GHz carrier frequency. The detected and amplified waveform is shown in Fig. 9. The input power and baseband frequency were −21 dBm and 1 kHz, respectively, and V_{CM2} was 0.75 V. A slow turn-off of the output was caused by the load in the oscilloscope (1-MΩ and 10-pF). Although the baseband signal was limited to 1 kbps due to the output load, the detector and amplifier had a simulated bandwidth of 100 kHz and could operate at 100 kbps when connected to the PWM CDR.

Figure 10 shows the output voltage of the detector and high-gain amplifier as a function of the input power. The measured and simulated characteristics were in good agreement. The output noise was measured with a spectrum analyzer. The results are shown in Fig. 11. The bit-error-rate (BER) was assumed to be 10^{-3}, which corresponded to the signal-to-noise ratio of 11 dB for amplitude-shift-keying (ASK). The sensitivity of the detector was calculated using [8]:

$$Sensitivity = \frac{3.5\left(\int N(f)df\right)^{1/2}}{\gamma}, \quad (1)$$

where $N(f)$ is the noise power density and γ is the conversion efficiency (output-voltage/input-power (V/W)). The calculated sensitivity values using Eq. (1) were −47.2 dBm (measurement) and −58.0 dBm (simulation). In the noise simulation, the wiring resistances in the power lines were taken into account. The difference between the two results might have been caused by unexpected on-chip effects (i.e., coupling between the input and output through the Si substrate) and/or unwanted noises in the experimental setup. The difference in the low-frequency region might have been caused by a threshold voltage variation of the fabricated MOSFETs.

The power consumption was 6.8 μW from a 1.5 V power supply. Table I compares the performance of our detector and amplifier with three wake-up receivers previously reported in literature.

Figure 12 shows the measured waveforms of the PWM input, the recovered clock, and the ring oscillator output. The rise timing of the clock corresponded to the center of the PWM time slot and the clock was successfully recovered. The oscillation frequency of the ring oscillator was 2.2 MHz. The clock recovery circuit operated correctly in the PWM bit-rate region from 200 bps to 500 kbps. About 4 seconds

(2^{23}/2.2 MHz) after the turn-off of the PWM signal, the recovered clock shut down. The power consumption of the clock recovery circuit was 15.7 μW when operated.

5. Conclusion

We developed a low-power wake-up receiver operating in the subthreshold region. The RF front-end of the detector and the high-gain amplifier and PWM clock recovery circuit were designed and fabricated using a 0.18-μm mixed signal/RF CMOS process with one poly and six metal layers. The sensitivity of the fabricated detector and high-gain amplifier was –48.7 dBm while consuming only 6.8 μW from a 1.5 V supply. The fabricated clock recovery circuit operated correctly in the PWM bit-rate region from 200 bps to 500 kbps.

Acknowledgments

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Figure captions

Fig. 1 Block diagram of wake-up receiver

Fig. 2 Envelope detector (M1 and M2) with offset cancellation (differential pair M3-M6 and C1)

Fig. 3 (a) Overview and (b) example timing chart of the PWM clock and data recovery circuit

Fig. 4 Analog front-end consisting of detector, high-gain amplifier, bias circuit (M8), passive RC filter, and LC matching circuit

Fig. 5 (a) Process corner simulation and (b) temperature effect of high-gain amplifier

Fig. 6 Fabricated detector and high-gain amplifier

Fig. 7 Fabricated PWM clock recovery circuit

Fig. 8 Measured input return loss

Fig. 9 Measured waveforms for input (lower trace) and output (upper trace)

Fig. 10 Comparison of measured and simulated output voltage versus input power

Fig. 11 Comparison of measured and simulated output noise

Fig. 12 Measured waveforms of input (uppermost trace), recovered clock (middle trace) and OSC output (lowermost trace) for (a) all “0” input and (b) all “1” input

Table I Comparison of fabricated detector with those reported in literature

	[3]	[5]*	[8]	This work
Type of work	Wake-up receiver	Wake-up receiver	Detector	Detector and amp.
Technology	90 nm CMOS	130 nm CMOS	–	180 nm CMOS
Frequency (GHz)	2	2.4	0.915	1.75
Power (μW)	52	19	20	6.8
Sensitivity (dBm)	–72	–50	–69	–47.2

* Simulation

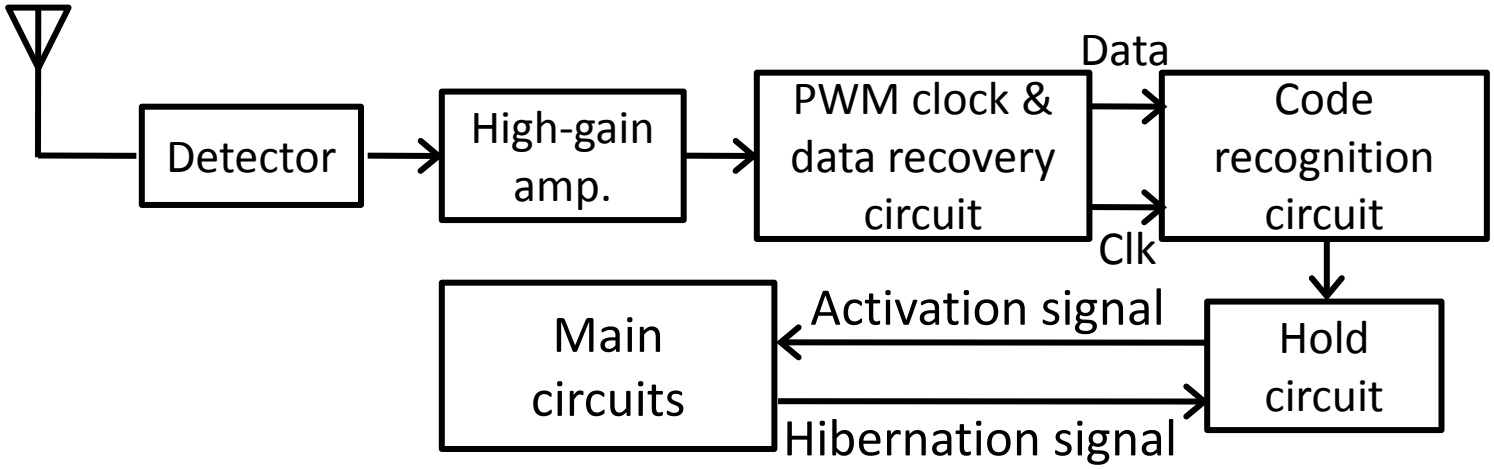

Detector
High-gain amp.
PWM clock & data recovery circuit
Data
Clk
Code recognition circuit
Hold circuit
Activation signal
Hibernation signal
Main circuits

Fig 1

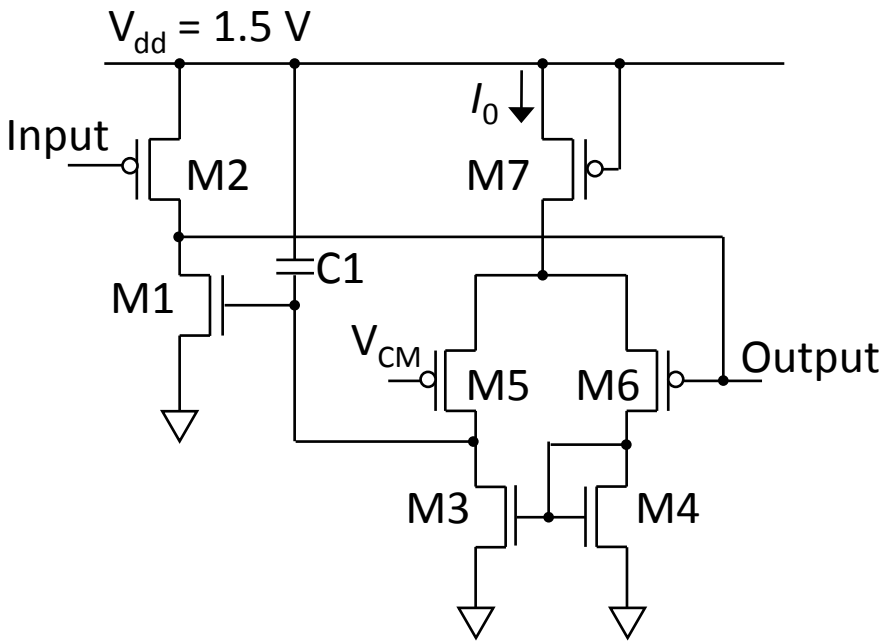


Fig 2

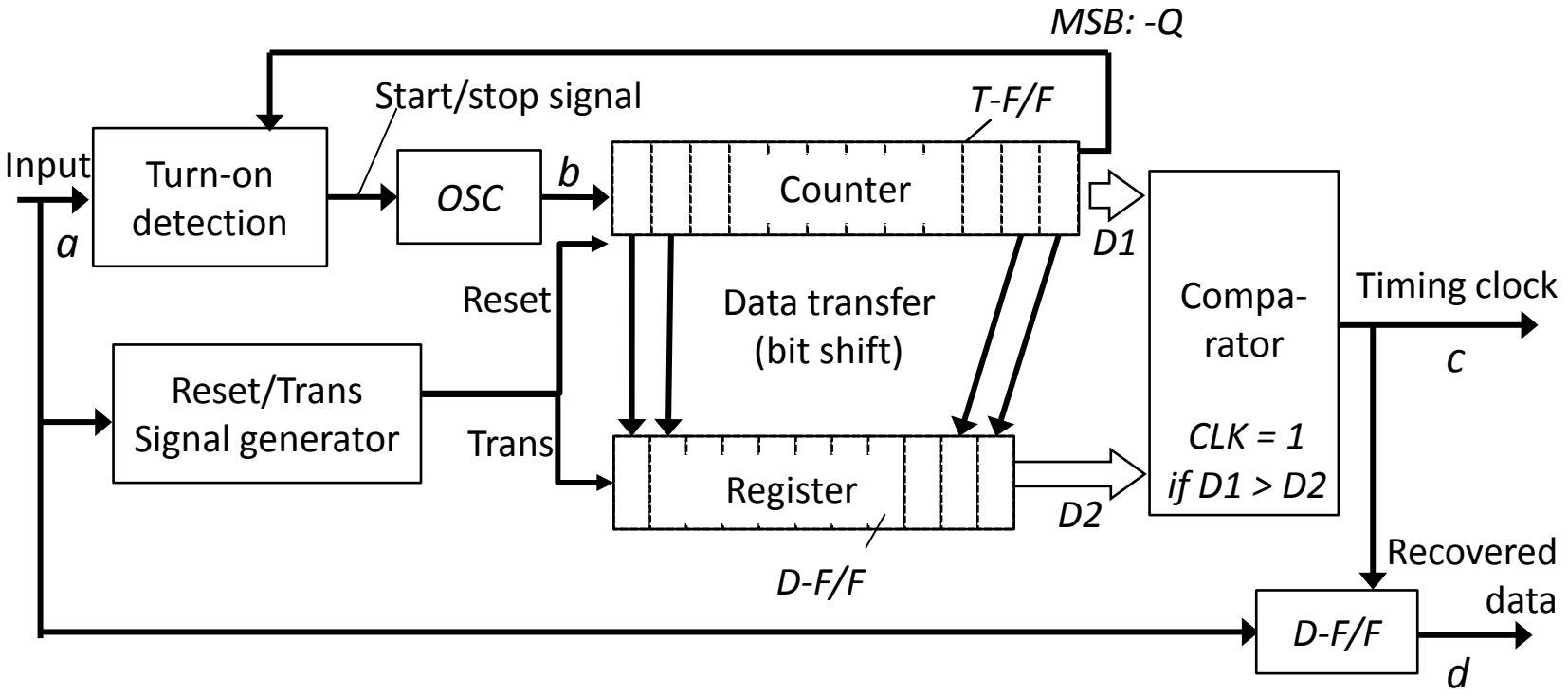

MSB: -Q
Start/stop signal
T-F/F
Input
Turn-on detection
OSC
b
Counter
a
D1
Reset
Data transfer (bit shift)
Compa-rator
Timing clock
c
Reset/Trans Signal generator
Trans
Register
CLK = 1 if D1 > D2
D2
D-F/F
Recovered data
D-F/F
d

Fig 3(a)

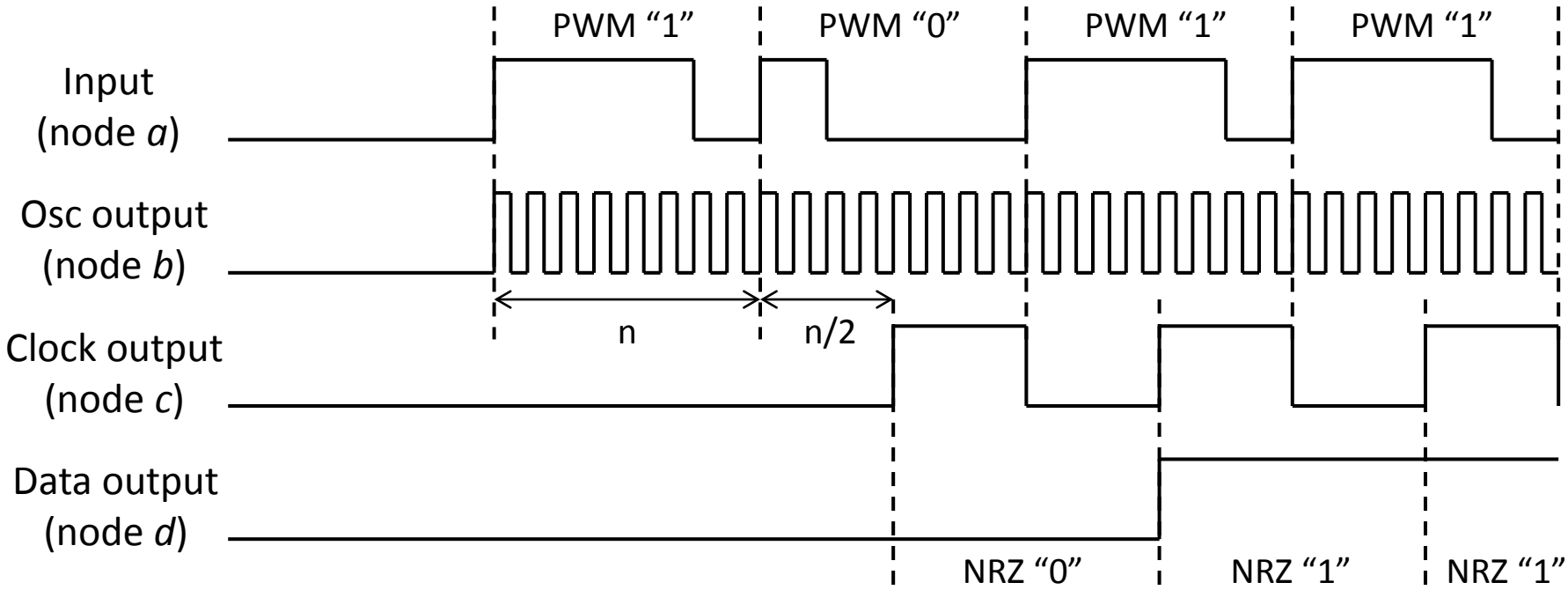

PWM “1”
PWM “0”
PWM “1”
PWM “1”
Input
(node *a*)
Osc output
(node *b*)
n
n/2
Clock output
(node *c*)
Data output
(node *d*)
NRZ “0”
NRZ “1”
NRZ “1”

Fig 3(b)

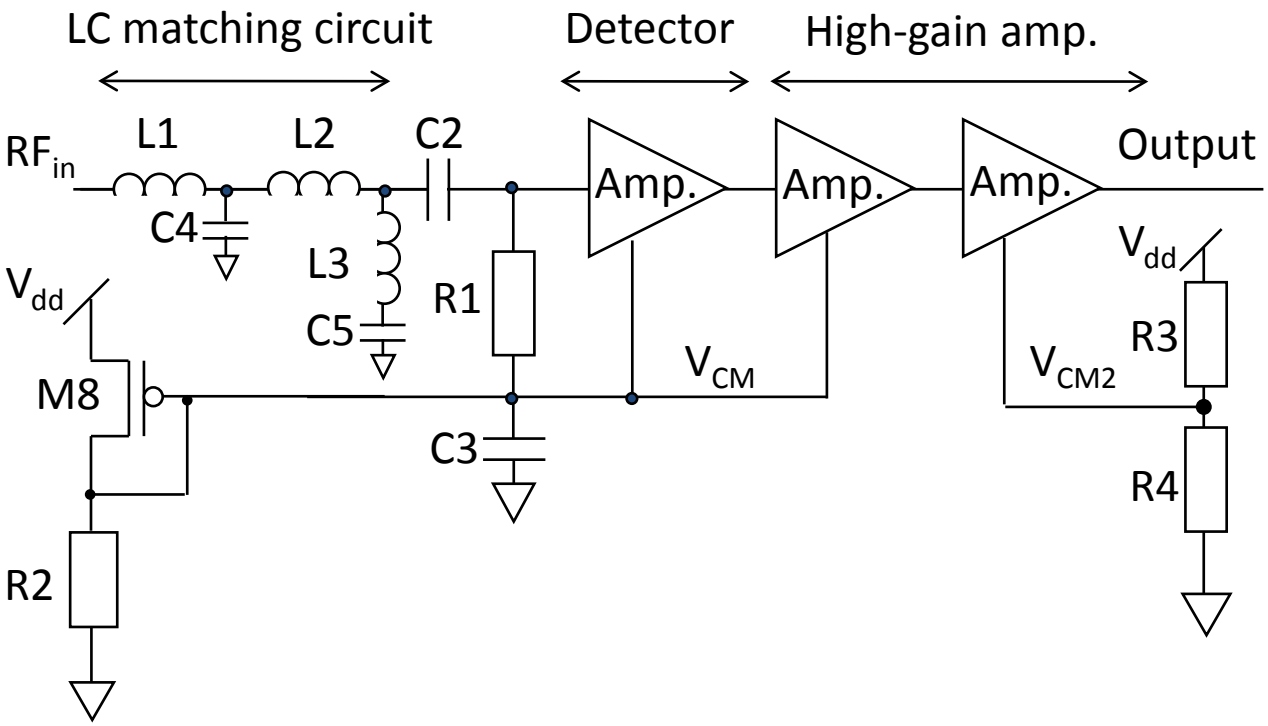
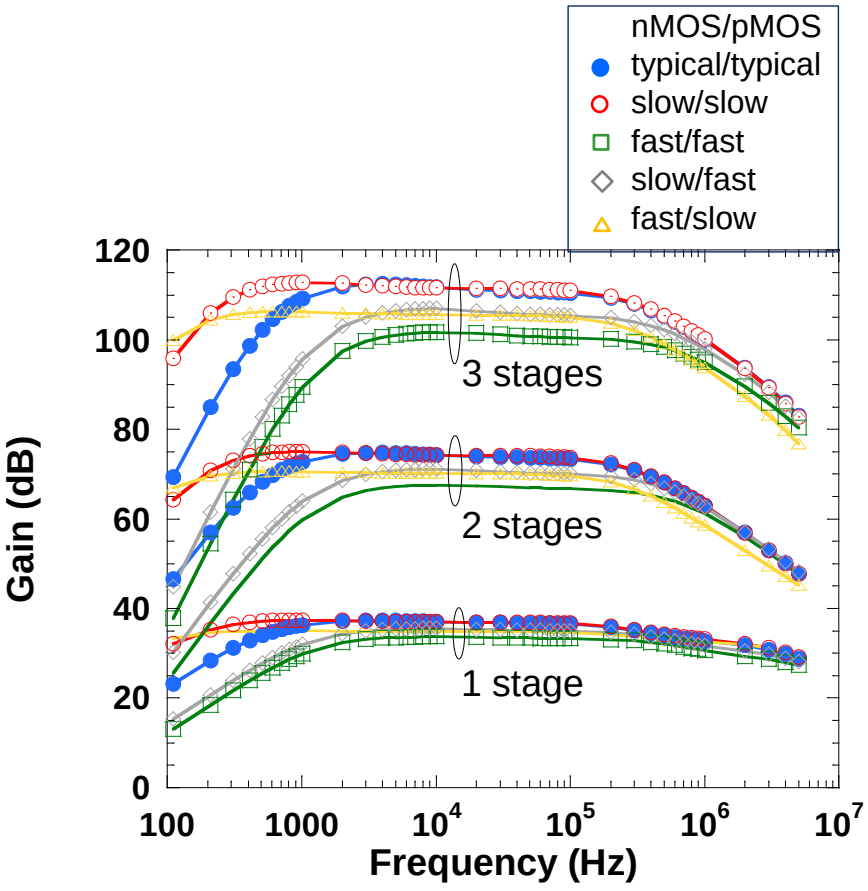
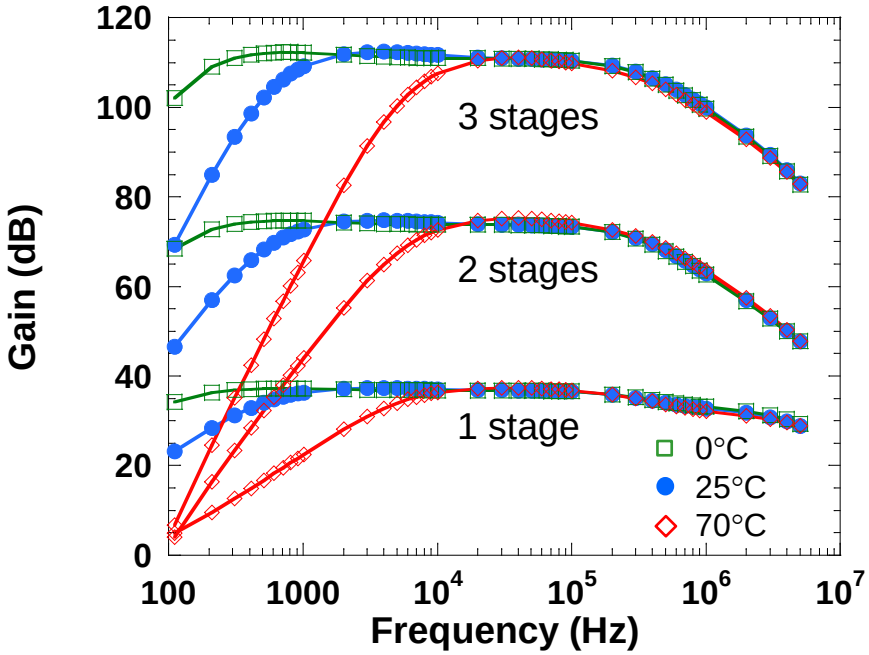

LC matching circuit
Detector
High-gain amp.
RF in
L1
L2
C2
C4
L3
C5
R1
Amp.
Amp.
Amp.
Output
V dd
M8
V CM
C3
V dd
R3
V CM2
R4
R2

Fig 4


nMOS/pMOS
typical/typical
slow/slow
fast/fast
slow/fast
fast/slow
3 stages
2 stages
1 stage
Gain (dB)
Frequency (Hz)
120
100
80
60
40
20
0
100
1000
10^4
10^5
10^6
10^7

(a)


3 stages
2 stages
1 stage
0°C
25°C
70°C
Gain (dB)
Frequency (Hz)
120
100
80
60
40
20
0
100
1000
10^4
10^5
10^6
10^7

(b)

Fig 5

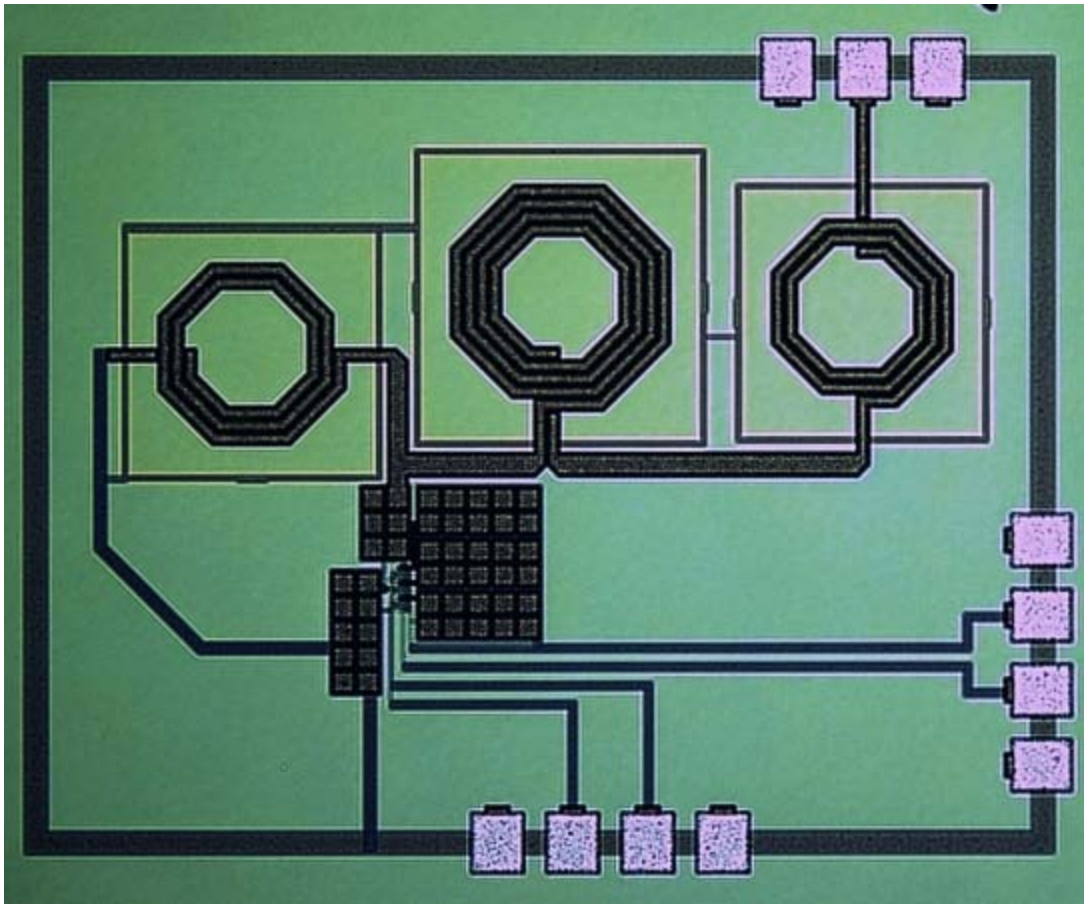


Fig 6

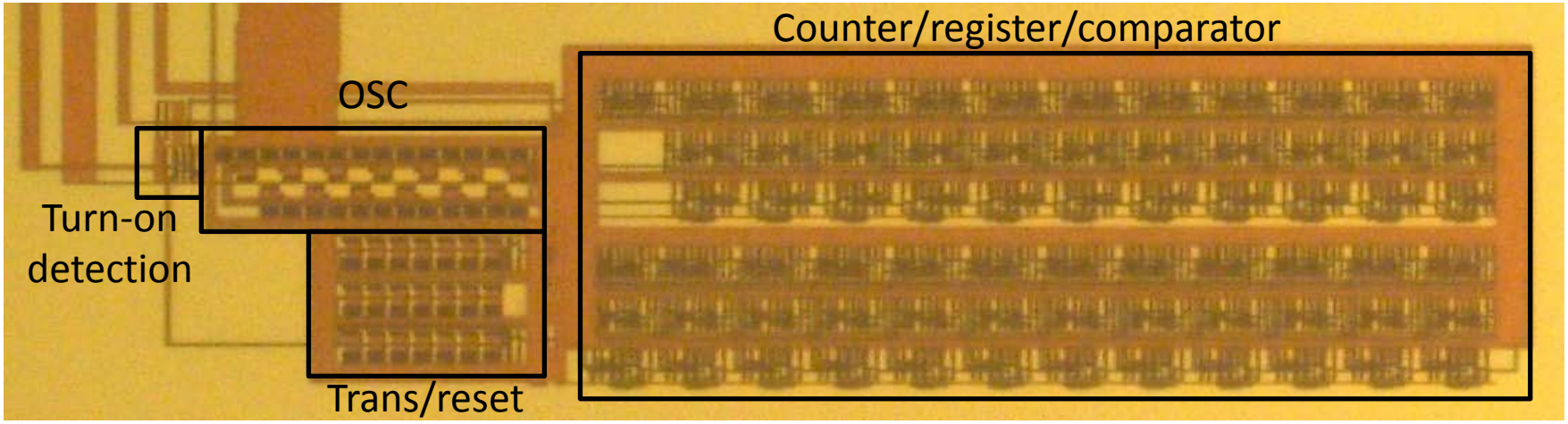

Counter/register/comparator
OSC
Turn-on
detection
Trans/reset

Fig 7

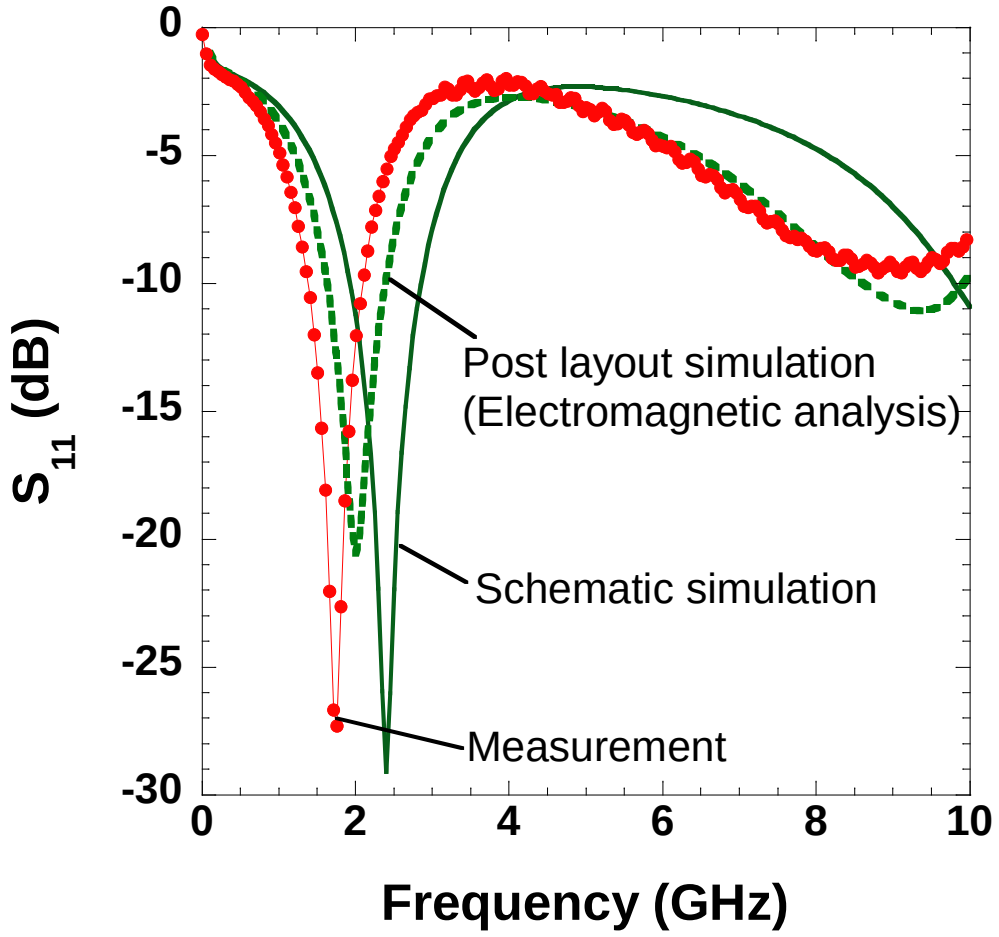

0
-5
-10
-15
-20
-25
-30
S11 (dB)
0
2
4
6
8
10
Frequency (GHz)
Post layout simulation
(Electromagnetic analysis)
Schematic simulation
Measurement

Fig 8

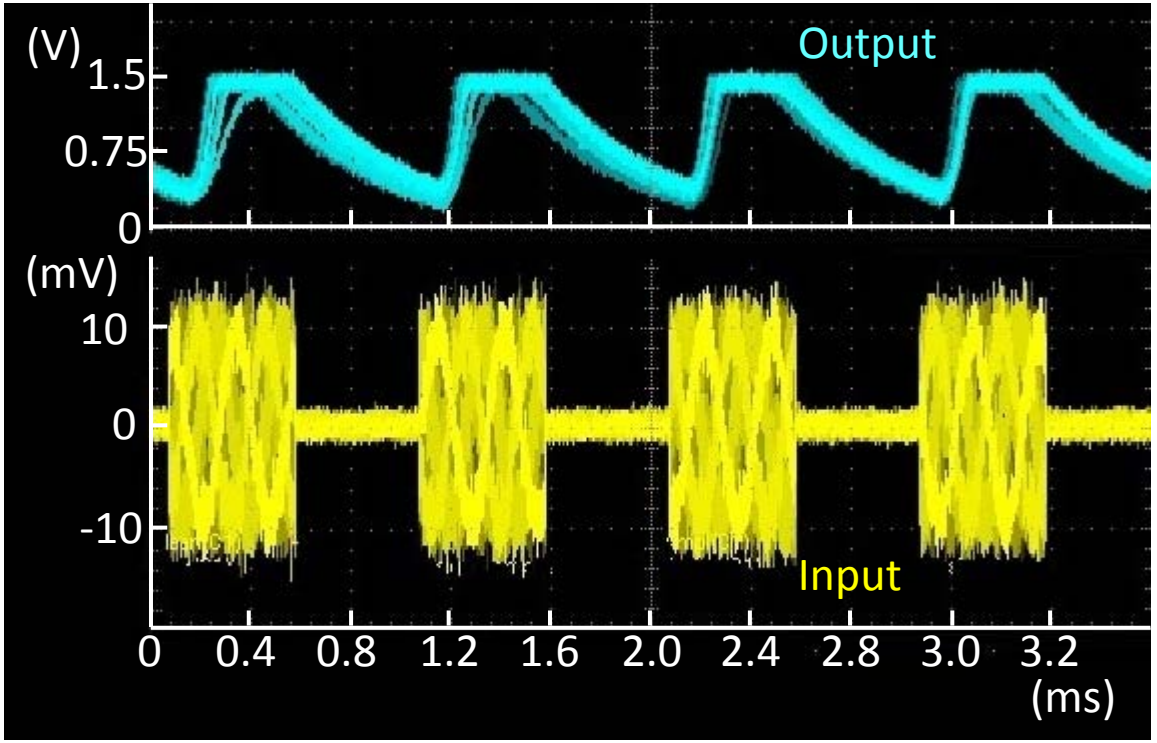


Fig 9

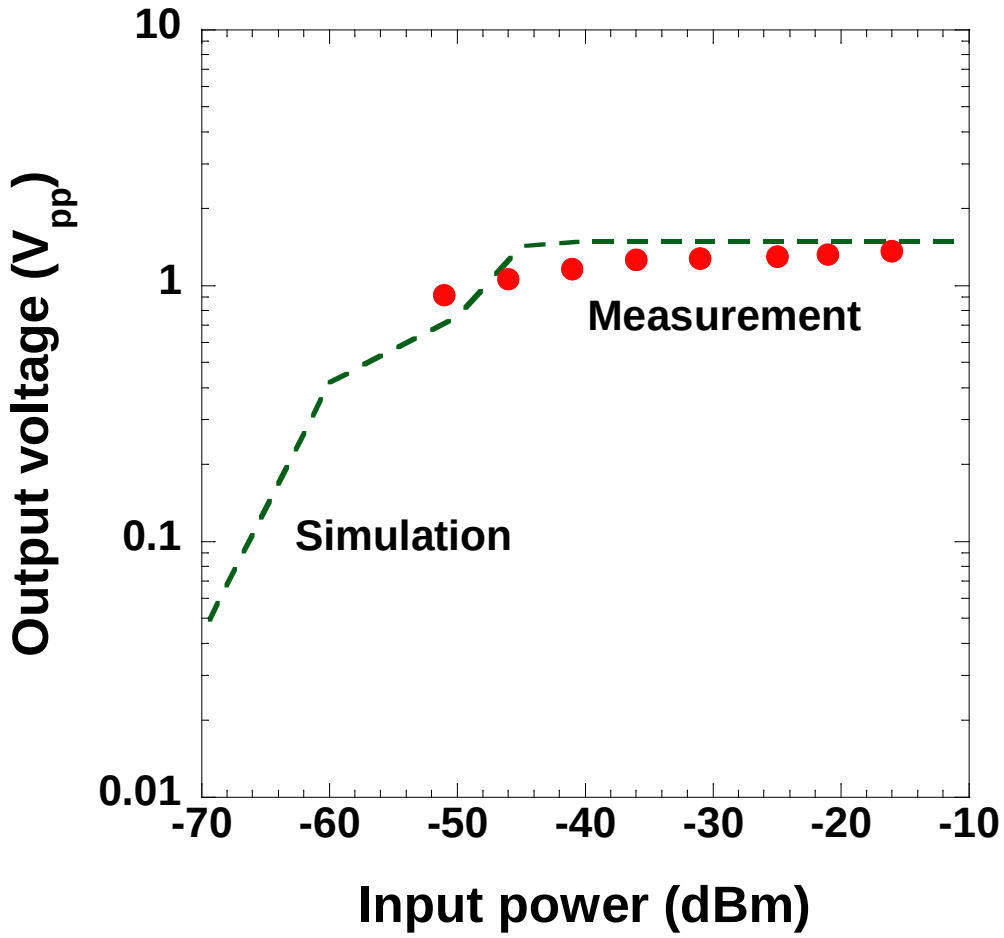

10
1
0.1
0.01
Output voltage (V_{pp})
-70
-60
-50
-40
-30
-20
-10
Input power (dBm)
Measurement
Simulation

Fig 10

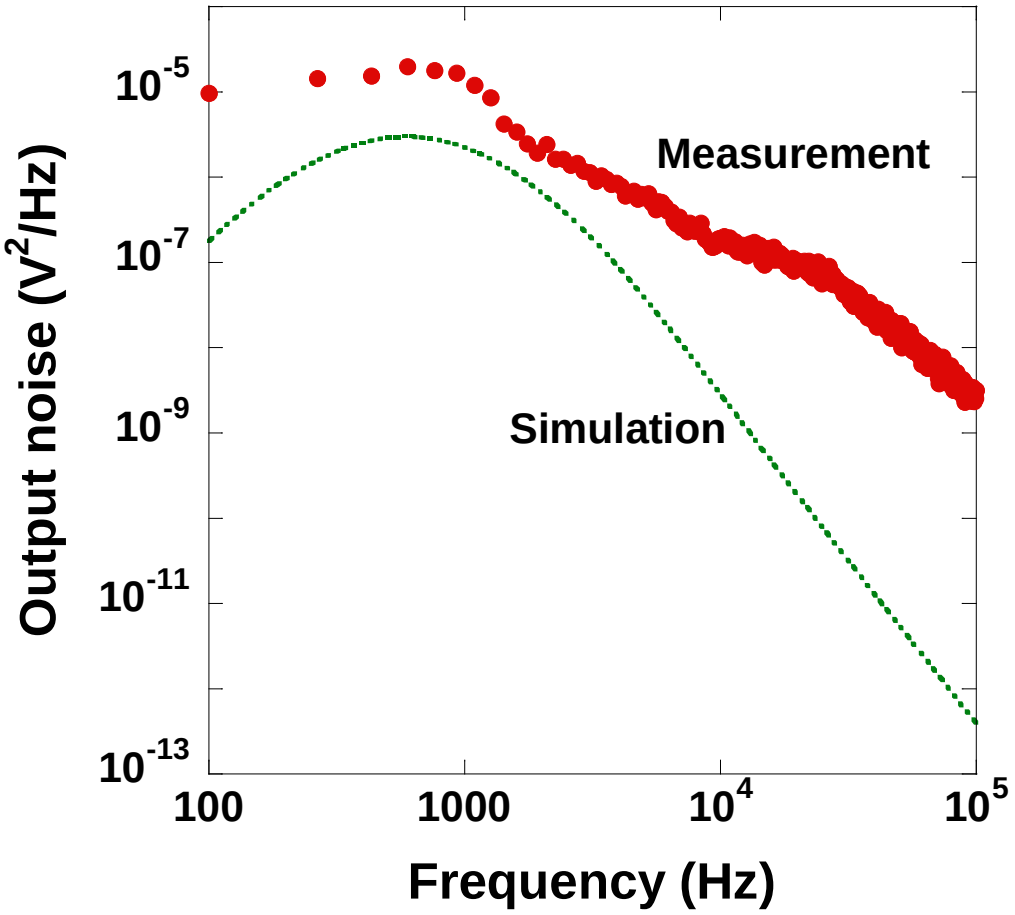
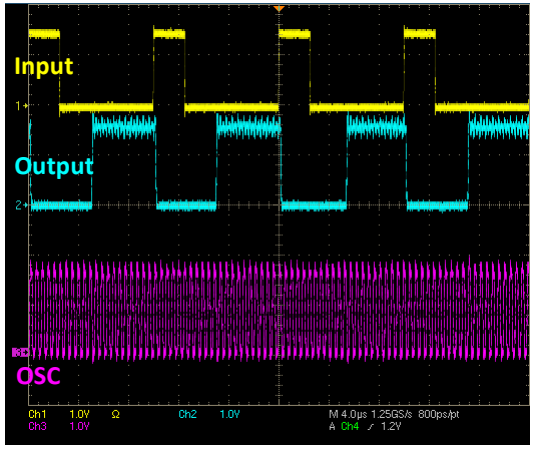

Output noise (V²/Hz)
10-5
10-7
10-9
10-11
10-13
Measurement
Simulation
100
1000
10⁴
10⁵
Frequency (Hz)

Fig 11


Input
Output
OSC
Ch1 1.0V Ω Ch2 1.0V M 4.0µs 1.25GS/s 800ps/pt
Ch3 1.0V A Ch4 ⟋ 1.2V

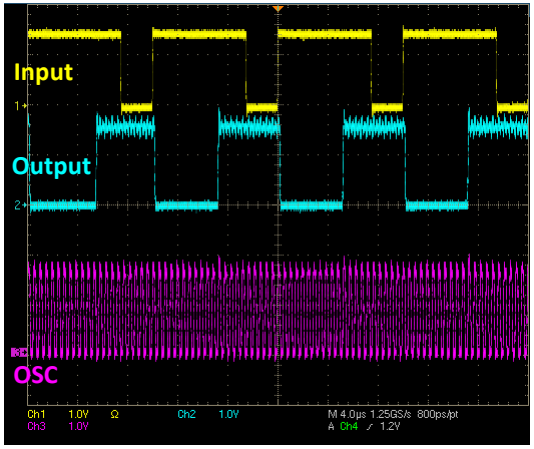

Input
Output
OSC
Ch1 1.0V Ω Ch2 1.0V M 4.0µs 1.25GS/s 800ps/pt
Ch3 1.0V A Ch4 ⟋ 1.2V

Fig 12